On-chip and In-package Antennas for mm-Wave CMOS Circuits

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***Abstract*—This paper discusses challenges, design issues and possible solutions to get mm-Wave signals off-chip. Simulation- and measurement results are discussed for three mm-Wave designs at different frequencies in bulk CMOS technology. (1) The design of a back-to-back IC-to-board interconnect using wire-bonding and microstrip lines is described to package and measure the chips without the need for a mm-Wave probe. (2) An on-chip antenna implementation at 540GHz in a 40nm CMOS technology with metal reflector is discussed. And (3) an on-chip collinear broadside array at 120GHz, also designed in a 40nm CMOS technology and flip-chipped on an alumina substrate is proposed as a possible solution.**

***Index Terms*—mm-Wave, CMOS, on-chip antenna, in-package antenna.**

I. Introduction

The increase in circuit operating frequency into the (sub) millimeter-wave (mm-Wave) spectrum poses some issues in getting the mm-Wave signals off-chip. The use of high-performance off-chip antennas is challenging due to the inter-chip connection losses, whereas wire-bonding between IC and board suffers from increased interconnect losses at mm-Wave frequencies. In the E-band frequency range, wire-bonding is still possible, which allows off-chip antennas. At even higher frequencies, the antenna size becomes small enough to be implemented on-chip, avoiding the interconnect losses. But the antenna performance is limited due to the lossy silicon substrate. Section II presents an IC-to-board interconnect for E-band applications (71-76GHz and 81-86GHz) using bondwires and microstrip lines. Section III discusses the implementation of two on-chip antennas, radiating respectively at 120GHz and 540GHz, in a 40nm bulk CMOS technology.

II. Millimeter-wave IC packaging and measurement with rectangular waveguide ports

An integrated on-chip antenna has limited performance because of the lossy silicon substrate. Also, for E-band applications, an on-chip antenna would occupy a large area corresponding to the wavelength. One solution is to design these bulky components on a PCB to reduce high antenna cost.

Bondwires can be used to get the mm-Wave signals off-chip [1], [2]. Wire-bonding has been widely used for the interconnection, which is simple, low-cost and well-established. However, for mm-Wave applications, the inductance of the bondwire becomes dominant and will influence the performance significantly. In this paper, we developed a simple wire-bonding interconnect between ICs and microstrip lines for E-band applications.

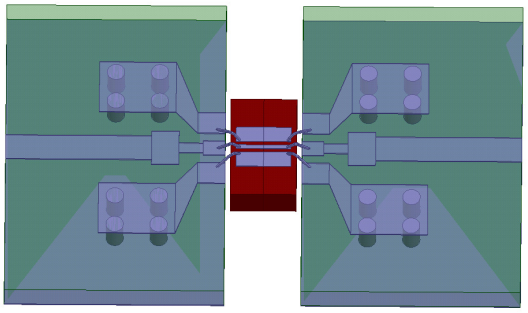


Fig. 1: Back-to-back bondwire interconnect through an on-chip 50Ω transmission line.

Figure 1 shows a back-to-back IC-to-board transition with bondwires. To reduce the length of the bondwires, a 700µm by 1300µm cavity is implemented on the alumina board and the chip is placed in this cavity. The height difference between chip and board is now only 22µm. There is a 50µm wide gap between chip and board, and another 50µm between bond

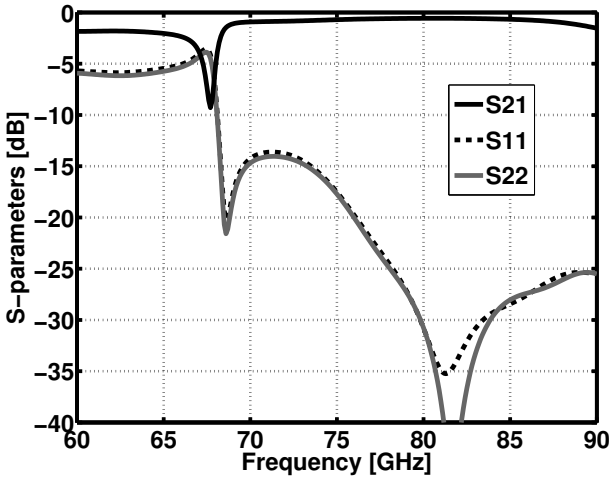
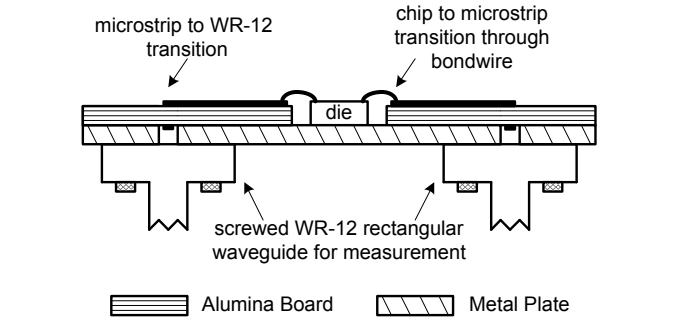


Fig. 2: S-parameter simulation results for back-to-back bondwire interconnect through an on-chip 50Ω transmission line.

pads and the edge of the chip. Taking everything into account, the total bondwire length is reduced to 240µm. A matching network, containing grounded vias and varying line widths, is used to compensate the inductance of the bondwires.

Figure 2 shows the simulated S-parameters results with a 50Ω transmission line. Return loss lower than -14dB is realized from 67GHz to over 90GHz. The average insertion loss is only 0.55dB.

The presented bondwire interface was used to package and measure the chips without using a mm-Wave probe. A transition between ICs and rectangular waveguides using bondwires is proposed, as illustrated in Figure 3. The WR-12 waveguide ports are fixed at the bottom of the alumina board. The working bandwidth is limited by the microstrip-to-waveguide transition, which is narrow compared to the bondwire interconnect.



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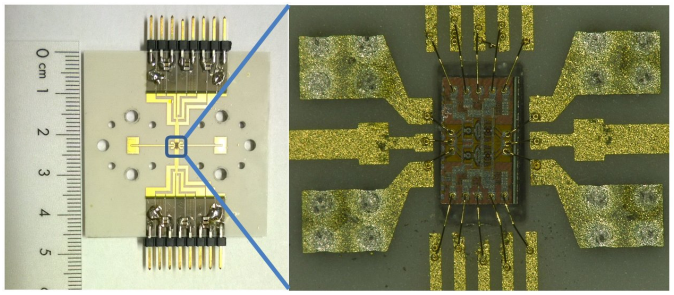


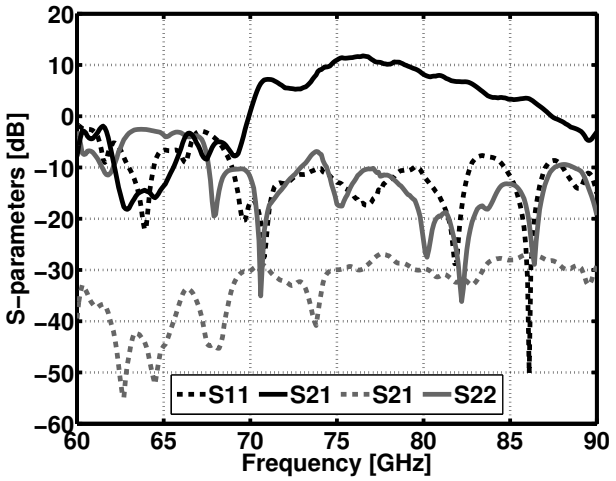
(b)

Fig. 3: (a) Cross-section view of the bondwire packaging with transition to WR-12 waveguide and (b) photograph of alumina substrate with wire-bonded power amplifier.

Measured results of a wire-bonded power amplifier (PA) chip with waveguide ports are shown in Figure 4. The maximum measured gain is 11.7dB including all the packaging losses, which is 2dB less than simulated. The maximum output power is 16.3dBm and peak drain efficiency is 20%. The performance is impacted by fabrication errors and misalignment between alumina board and WR-12 waveguide.

III. On-chip antenna in CMOS

Two on-chip antenna implementations are discussed in this paper, sections III-B and III-C present one at 540GHz and one 120GHz respectively.



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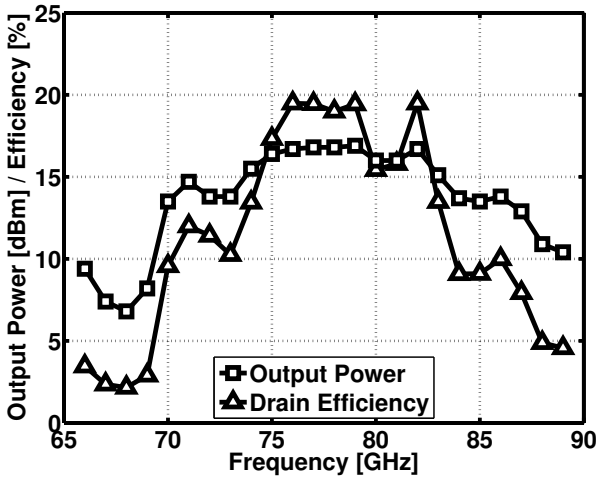

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Fig. 4: (a) Measured S-parameter results of bondwire packaged PA and (b) measured output power and drain efficiency of packaged power amplifier.

A. On-chip antenna introduction

The major drawbacks of on-chip antennas are the lossy substrate and the backside radiation. Thinner substrates would improve this, but would require unpractical thin substrates at mm-Wave frequencies [3]. To recover the radiation in the silicon substrate, a metal reflector can be used to reflect the backwards radiated signal and add it to the upwards radiated signal. Due to this reflector forward radiation is enhanced, which allows normal bonding and packaging procedures.

The distance between the antenna and the reflector is critical to ensure constructive interference. This can only be obtained when both the reflected and original wave have the same phase. In other words, the traveled path should be an odd multiple of $\lambda/2$. The reflected wave undergoes a 180 degrees ($\lambda/2$) phase shift at the point of reflection, so the path length should cover the remaining 180 degrees ($\lambda/2$) phase shift.

Varying the substrate thickness can set this antenna-to-reflector distance. In Section III-B, the substrate thickness refers to the CMOS substrate, while in Section III-C the alumina substrate thickness is the critical variable. Both implementations make use of a reflector to enhance radiation in the desired direction. The reflected waves pass trough the integrated circuit without interfering with on-chip passives and circuit operation.

B. On-chip antenna at 540GHz

For THz signal generators, fully integrated antennas can be realized on-chip as the wavelength λ is smaller than 1 millimeter. A signal source, implemented in a 40nm CMOS technology, generates a differential 540GHz signal [4](third harmonic of a 180GHz fundamental) which is radiated off-chip using an antenna. Since process variations can have a large impact on the operating frequency of THz sources, an antenna with broad bandwidth is required. Strict design rules in nanometer CMOS call for an antenna type which is compatible with the available metal stack and layout restrictions.

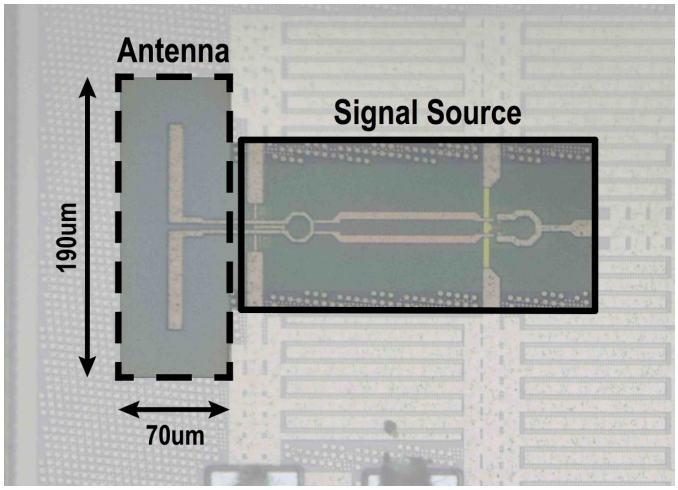


Fig. 5: Die photograph of the integrated dipole antenna, designed to radiate a 540GHz signal.

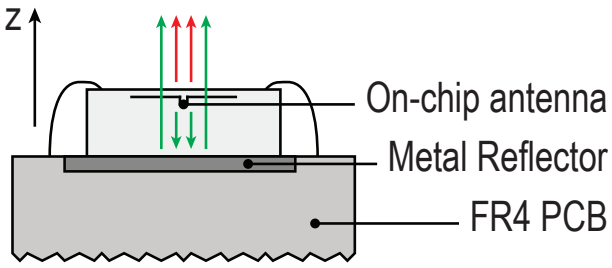


Fig. 6: Cross-section view of IC with on-chip dipole antenna wire-bonded on an FR4 PCB with metal reflector.

Patch antennas for THz radiation have been fabricated using the top- and bottom metals of the CMOS process [5]. The reflector in the lower metals shields the patch from the lossy Si-substrate, increasing radiation efficiency and directivity. The downside is the single-ended feed and narrow bandwidth. Due to the differential signal and the preference for a broader bandwidth, a half-wavelength dipole antenna with increased trace width is implemented on-chip in the top metal layer of the CMOS process, of which a die photo is shown in Figure 5.

Figure 6 shows the implementation of the metal reflector placed on the FR4 PCB onto which the silicon chip is mounted. The foundry's default 12mil (305µm) substrate thickness allows constructive interference of the reflected signal, as mentioned earlier, without compromising the mechanical strength of the silicon die.

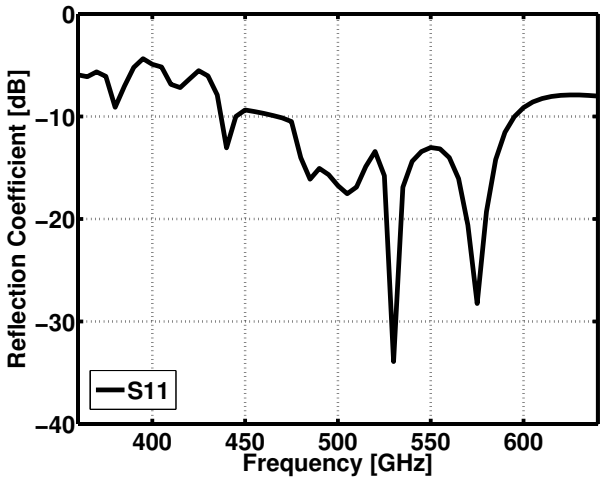
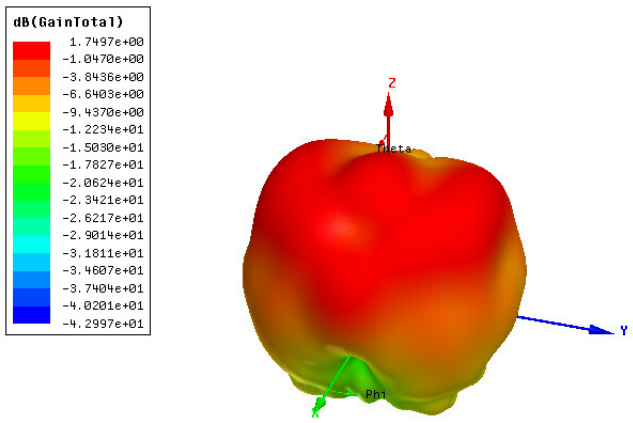


Fig. 7: Simulated reflection coefficient of the on-chip dipole antenna with reflector.

The simulated reflection coefficient (Figure 7) shows a low S11 over a broad frequency bandwidth around the desired third harmonic signal. Due to the differential nature of the signal source, the unwanted second and fourth harmonic signal are suppressed. Simulations using ANSYS HFSS show a peak gain of 1.75dBi (Figure 8a) and a radiation efficiency of 19%. The radiation patterns in the E- and H-plane of the antenna (Figure 8b), driven by the on-chip signal source, were measured using a down-converter with WR1.5 horn antenna and a R&S FSU Spectrum Analyzer. This shows the feasibility of on-chip antennas for THz applications, integrated with the driving electronic circuits in nanometer CMOS. No complex packaging process or bulky external components or lenses are needed to get the THz signal off-chip.

C. On-chip collinear broadside array at 120GHz

The challenge in this design is to bring the 120GHz signal off-chip. An on-chip bondwire antenna has been used in [6] at this frequency. This work presents an improved integrated antenna, which eliminates the bondwire shape inaccuracy and results in a more reliable solution towards packaging and fabrication. The two main contributions are (1) making use of an antenna array, which results in a more directive radiation



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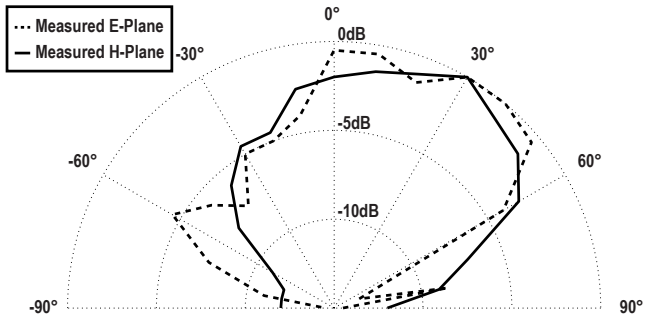

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Fig. 8: Simulated gain (a) and measured radiation pattern (b) of the 540GHz on-chip dipole antenna.

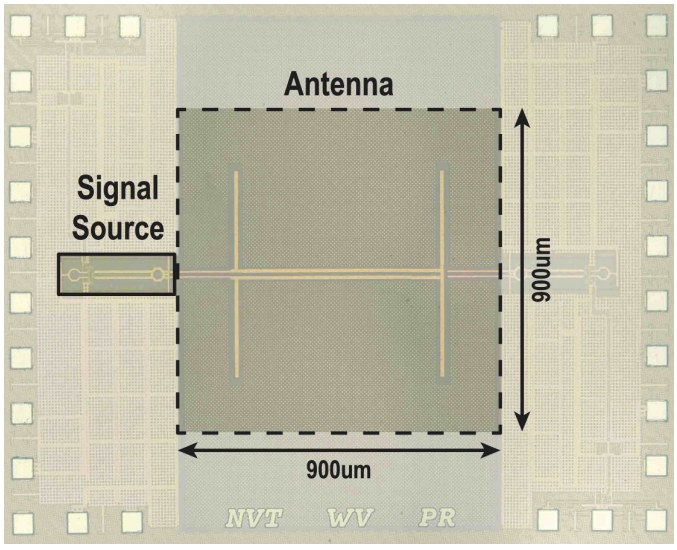


Fig. 9: Die micrograph of on-chip collinear broadside array.

pattern and (2) the use of a flip-chip packaging technique combined with an off-chip reflector to enhance the radiation in the positive z-direction.

An on-chip collinear broadside array with backside radiation is proposed as an on-chip solution for transmitting the 120GHz modulated signal. The carrier signal is generated on-chip and frequency modulation is applied for communication purposes.

The wavelength of the 120GHz wave is approximately 810µm in the alumina (Al_2O_3, ϵ = 9.5) substrate for the flip-chip packaging. The antenna, of which a die photograph is shown in Figure 9, is designed in the top metal layer of the CMOS stack to minimize the parasitic resistance and capacitive coupling to the CMOS substrate. By using the flip-chip packaging technique, the 12mil thick die is placed upside down, which allows backward substrate radiation in the positive z-direction.

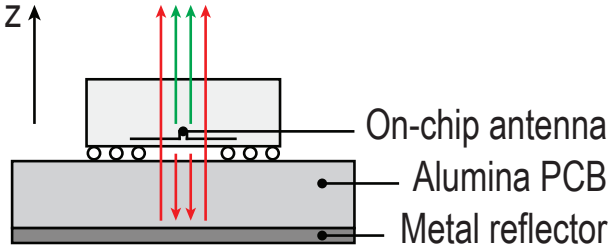


Fig. 10: Cross-section view of IC with on-chip dipole antenna array flip-chipped on an alumina PCB with metal reflector.

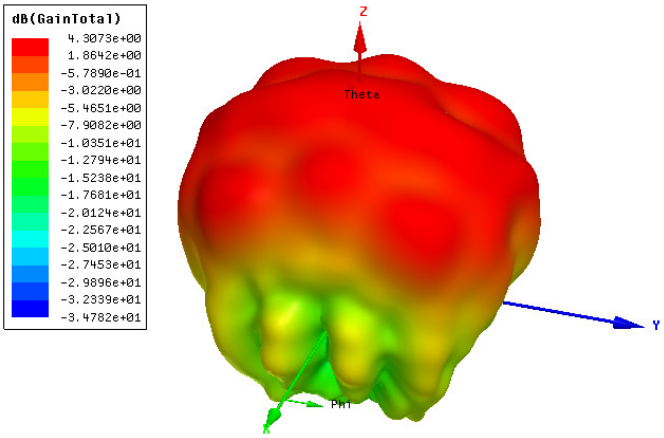
As illustrated in Figure 10, a metal reflector at the bottom of the alumina substrate is used to reflect the downwards (negative z-direction) radiated wave. An ideal thickness of $\lambda/4$ (203µm) is calculated. Due to the standardized alumina substrates, a thickness of 10mil (254µm) is used in this design.

The simulation result of the far field antenna radiation pattern is depicted in Figure 11a. The EM simulations are performed with ANSYS HFSS. A simulated radiation efficiency of 45% and a 4.3dBi peak gain is achieved with an on-chip collinear broadside array. To measure the E-plane and H-plane radiation pattern, a WR-8 horn antenna with down-converter was used to measure the radiated power with a R&S FSW Spectrum Analyzer. The measured E- and H-plane are presented in Figure 11b.

Figure 12 shows the simulated S11-curve with a minimized value around 120GHz.

IV. Conclusion

This work demonstrates several techniques to get mm-wave signals off-chip. For E-band applications, an IC-to-board packaging solution is presented using wire-bonding and microstrip lines. This gets the mm-wave signals off-chip without needing probes. For higher frequencies, two on-chip antennas are implemented in a 40nm CMOS technology and discussed: a dipole radiating at 540GHz with reflector below



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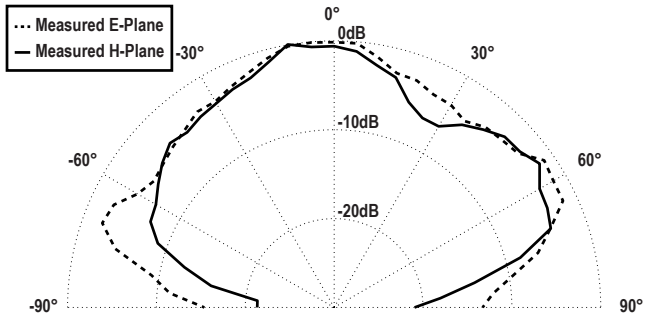

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Fig. 11: (a) Simulated gain and (b) measured and normalized E-plane and H-plane radiation pattern of the on-chip collinear broadside array at 120GHz.

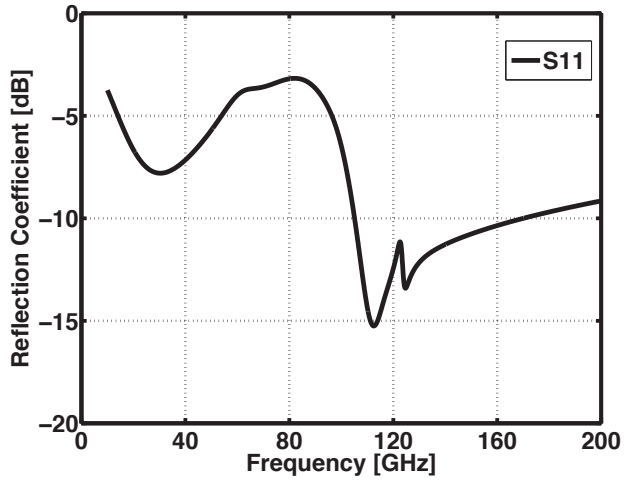

Fig. 12: Simulated reflection coefficient of the on-chip collinear broadside array with reflector.

the Si-substrate, and a flip-chipped collinear broadside array radiating at 120GHz through the backside of the substrate.

REFERENCES

[1] Y. Zhang, D. Zhao, and P. Reynaert., "Millimeter-wave packaging on alumina board for e-band cmos power amplifiers." in *Power Amplifiers for Wireless and Radio Applications (PAWR), IEEE Topical Conference on. IEEE*, 2015.

[2] G. Liu, A. Trasser, A. Ulusoy, and H. Schumacher, "Low-loss, low-cost, ic-to-board bondwire interconnects for millimeter-wave applications," in *Microwave Symposium Digest (MTT), IEEE MTT-S International*, June 2011, pp. 1–4.

[3] G. Rebeiz, "Millimeter-wave and terahertz integrated circuit antennas," *Proceedings of the IEEE*, vol. 80, no. 11, pp. 1748–1770, Nov 1992.

[4] W. Steyaert and P. Reynaert, "A 0.54 thz signal generator in 40 nm bulk cmos with 22 ghz tuning range," in *ESSCIRC (ESSCIRC), 2013 Proceedings of the*, Sept 2013, pp. 411–414.

[5] E. Seok, C. Cao, D. Shim, D. Arenas, D. Tanner, C.-M. Hung, and K. O, "A 410GHz CMOS Push-Push Oscillator with an On-Chip Patch Antenna," in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, 2008, pp. 472–629.

[6] N. Deferm and P. Reynaert, "Design, simulation and measurement of a 120ghz on-chip antenna in 45nm cmos for high-speed short-range wireless connectors," in *Antennas Propagation (ISAP), 2013 Proceedings of the International Symposium on*, vol. 01, Oct 2013, pp. 645–648.